IN THE CLAIMS

1. (Original) A multi-issue processor comprising:

- a plurality of issue slots, each one of the plurality of issue slots comprising a plurality of functional units and a plurality of holdable registers, the plurality of issue slots comprising a first set of issue slots and a second set of issue slots; and
- a register file accessible by the plurality of issue slots;

characterized in that a location of at least a part of the plurality of holdable registers in the first set of issue slots is different from a location of at least a corresponding part of the plurality of holdable registers in the second set of issue slots.

2. (Original) A multi-issue processor according to Claim 1 comprising:

- a first instruction set means having access to at least the first set of issue slots;
- a second instruction set means having access to the second set of issue slots.

3. (Currently amended) A multi-issue processor according to Claim 1 ~~or 2~~ wherein:

in the first set of issue slots the location of the plurality of holdable data registers is at individual data inputs of the functional units, while in the second set of issue slots the location of the plurality of holdable data registers is at common data inputs of the functional units.